PATENT IBM Docket No. FR920010005US1

#### REMARKS

This amendment is in response to the Office Action mailed August 12, 2004.

#### A. RESTRICTION REQUIREMENT

Applicants affirm election of claims 1-9, 12, 13 and 15-18 (Group I.) for examination.

Applicants traverse the Group II. (claims 10 and 14) and Group III. (claims 11 and 14) restriction. By the Examiner's own admission the classification for the claims of both groups are the same (i.e. class 708, subclass 492). The claims of both groups are sufficiently close so the Examiner only has to search a single class and subclass for relevant prior art. To restrict these claims when only a single class and subclass has to be searched would be equivalent to putting form over substance. As a consequence, restriction for examination purposes as suggested by the Examiner appears to be improper. Applicants request claims 10, 11 and 14 be examined as a single group.

#### **B. DRAWINGS**

The Examiner objects to Figures 7, 11 and 13 because numerals on these figures are not mentioned in the description. Except for numeral 1100, Figure 11, which is already mentioned at page 17, line1, applicants' specification, the specification is amended to refer to the named numerals, set forth on page 4 of the Office Action.

PATENT IBM Docket No. FR920010006US1

### C. SPECIFICATION

The Examiner objects to the Abstract because it exceeds 150 words. In response, a new Abstract, conforming to Patent Office Rules for abstract, is submitted herewith.

With respect to claim 1 the Examiner states: "displacing in said multiplicative cyclic group a current value of said d-bit wide FCS, considered as one of said d-bit wide binary vectors of a value corresponding to said N-bit at a time" is objected to because it is not taught in the specification.

In response, applicants believe there are sufficient teachings of "displacing in said multiplicative cyclic group" within specification. For example, the attention of the Examiner is directed to the description of Figure 11 especially item 1120, page 17, lines 15-20, Summary of the Invention, etc. We believe the referred portion represents sufficient teaching of displacing in said multiplicative cyclic group.

Regarding claim 4 the Examiner states: "handling directly said new N-bit chunk of data bits as if it is said d-bit wide division results". According to the Examiner, nowhere does the applicant teach "handling directly said new bit chunk of data bit as if it is said d-bit wide division results". For teaching of this phrase, the attention of the Examiner is directed to Figure 6, element 630 and the portion of the specification describing Figure 6 and Figure 5, element 535 and the portion of the specification describing Figure 5.

#### D. CLAIM OBJECTIONS

Claims 1-9, 12, 13 and 15-18 are objected to because they contain reference numbers to the drawings. According to the Examiner they should be removed. Applicants respectfully disagree with the Examiner on this point. Applicants believe that the reference

# PATENT IBM Docket No. FR920010006US1

number makes it easier for the reader to associate the claim with both the drawing and the specification. The reference numbers are enclosed in brackets which clearly shows that they are not part of the claim. Applicants have no knowledge of any rule or Patent Office custom that prohibits such usage in the claim. If the Examiner still persists that the reference number should be removed applicants, respectfully, request the Examiner to identify the authority or rule that makes such requirement mandatory.

Claims 12, 13 and 15 are objected to as being in improper form because a multiple dependent claim cannot depend from another multiple dependent claim.

In response, the claims have been amended to remove multiple dependency.

The Examiner states his objection to claim 17 as follows: "Claim 17 recites, "in acts (d) being the calculated CRC" an act is not a calculated CRC." We believe the Examiner focus on only a portion of the claim gives rise to the misinterpretation that is applied. When the entire 17(g) is read it is believed that a reasonable interpretation is that the result being the calculated CRC and not the acts as the Examiner seems to suggest. As a consequence, we believe the language of the claim is proper as is and see no reason to amend at this point.

#### E. CLAIM REJECTIONS

Claims 1-9, 12, 13 and 15 are rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. In particular, and with respect to claim 1, the Examiner states: "displacing in said multiplicative cyclic group, a current value of said d-bit wide FCS, considered as one of said d-bit wide binary vectors of a value corresponding to said n-bit at a time". According to the Examiner nowhere in the specification does the applicant teach "displacing in said multiplicative cyclic group".

### PATENT IBM Docket No. FR920010006US1

Contrary to this statement "displacing in said multiplicative cyclic group" is taught in the specification in relation with the xN multiplier or multiplying step:

- Reference (560) in Fig. 5 page 12, lines 3 through 13.
- Figure 6 the 8x8 matrix is the xN multiplier of Figure 5: in description of Figure 6, page 13, lines 4-21.
  - Reference 1120 in Figure 11, page 17, lines 1-24.

To advance prosecution of this application, the language is amended as shown above.

Regarding claim 4 the Examiner states that "handling directly said new n-bit chunk of data bits as if it is said d-bit wide division result" is not taught in applicants' specification.

Contrary to the Examiner's position applicants believe that there is ample teaching in the specification. The description of this particular embodiment is included, for instance, in the description of Figure 5, page 11, lines 6-15 for the explanation that a dividing step is only necessary if N is greater than d. To promote prosecution of this application claim 4 is modified as shown above.

With respect to claim 6 the Examiner states that nowhere does applicants define "forward multiplication". Forward multiplication relates to the direction relative to the bit stream for which the CRC calculation is taken. When the CRC is computed starting from the most significant bit such as 530 Fig. 5 the multiplication shown in step 560 Fig. 5 is referred to as the forward multiplication. Applicants direct the attention of the Examiner to Fig. 5, element 560, and the description set forth on page 11, line 23 through page 12, line 29. In addition, applicants have amended page 12 to state "this multiplication [560] is termed forward multiplication". It is believed that this amendment is not new matter because applicants can amend the specification with information shown in the drawings and recited

PATENT IBM Docket No. FR920010006US1

in the claims. In addition, applicants argue that the language in the claim need not track the description in the specification word for word. Providing the language used in the claim can be associated with the specification, the requirement of 35 USC 112, first paragraph is met.

Regarding claim 7 the Examiner argues backward multiplication is not defined.

In response and with reference to arguments supporting the rejection of claim 6 backward multiplication depends on whether the CRC is calculated starting from the least significant bit in the binary string. This concept is shown in Fig. 7 element 760 and described at page 15, lines 1-10, applicants' specification. It is noted that in line 9 of page 15 the concept of forward multiplier relative to Fig. 5 is described. This again supports applicants' position that forward multiplication is described in the specification. Like the amendment to Figure 5 applicants add the sentence "this multiplication [760] is termed backward multiplication". As argued relative to Fig. 5 this amendment is permissible since it is shown in the drawings, discussed in the specification and recited in the claims.

Regarding claims 16-18 the Examiner argues "displaying in a multiplicative cyclic group" is not taught in the specification.

In response, applicants wish to point out that displaying should have been displacing. The claim should have read "displacing in a multiplicative cyclic group . . . ". This element of the claims is common to claim 1. Therefore, the arguments provided in claim 1 to show support in the specification is equally applicable and incorporated herein by reference. In order to advance prosecution claim 16 is amended as shown above.

# PATENT IBM Docket No. FR920010006US1

## F. REJECTION UNDER 35 USC 112, SECOND PARAGRAPH

Claims 1-9, 12, 13 and 15-18 are rejected under 35 USC 112, second paragraph, as being indefinite for failing for particularly point out and distinctly claim the subject matter which applicants regard as the invention. With respect to claim 1, the Examiner seems to raise issue with displacing as used in the claim. Claim 1 is amended as shown above and the issue which the Examiner raised is now moot. However, one point in the Examiner's argument that applicants would like to address relates to the Examiner's statement that displacement is not normally a group operation. Applicants are not sure of the context in which the Examiner is making this statement, but in the Galois field world which is a world of the cyclic redundancy check generation standard to which this invention belongs displacement is generally use and is a word of art. Displacement relates to a movement from one element of the cyclic group to another within the group.

Claims 1-9, 12, 13 and 15-18 are rejected under 35 USC 112; second paragraph, as being incomplete for omitting essential structural cooperative relationship of elements. In particular, the Examiner takes issue with "a current value of said d-bit wide FCS". In view of the amendment to claim 1 the phrase which the Examiner takes issue with is no longer in the claim. Therefore, the rejection is now moot.

Still referring to claim 1 the Examiner raised issues regarding "calculation" as used in claim 1. In response, the claim is amended to remove "calculation loop". As a consequence the issue is now moot.

Regarding claim 4 it has been amended as set forth above. Therefore, the issue which the Examiner raised relative to claim 4 is now moot.

PATENT IBM Docket No. FR9200100060S1

Claims 16-18 are rejected under 35 USC 112, second paragraph. The argument set forth by the Examiner in supporting the rejection is on page 10 of the Office Action. In response, claim 16 is amended as shown above. As a result of this amendment the argument which the Examiner presents to support the rejection is now moot.

#### Claim Rejection Under 35 USC 103

Claims 1-4, 6, 8, 9 and 16-18 are rejected under 35 USC 103(a) as being unpatentable over Cassidy, Daniel R. et al. (U.S. Patent Number 6,684,363 B1 in view of Wicker (Steven B. Wicker, "Error control system for digital communication storage" Princess Hall, 1995, pages 116-121).

Applicants, respectfully, traverse the rejection and argue the Examiner has not presented a prima facie case of obviousness as is required. Therefore, the claims are not obvious. To make out a prima facie case of obviousness, among other things, the combined references must teach all elements and limitations of the claimed invention. In addition, motivation to combine the references must be suggested in at least one of the references or the Examiner presents concrete and logical arguments as to why an artisan viewing the references would combine them in such a way to render the claimed invention obvious. For reasons set forth herein we believe the Examiner has not met his burden of presenting the prima facie case of obviousness. Therefore, the claims are not obvious.

# G. COMBINED REFERENCES DO NOT TEACH ALL ELEMENTS OF CLAIMED INVENTION

Claims 1 and 16, among other things, call for (a) generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors and (b) adding modular 2, said d-bit wide division result and said FCS so obtained.

# PATENT IBM Docket No. FR920010006US1

U.S. Patent No. 6,684,363 B1, the primary reference, describes system and method for calculating CRC using a table of CRC values in combination with a logical grid to quickly determine an appropriate CRC. Column 3, lines 24-53; Figures 5, 6 and 7; column 6, line 42 through column 7, line 32. Nowhere in Cassidy et al. or Steven B. Wicker reference are suggestions or reference of the elements (a) and/or (b) set forth in applicants' claim. As a consequence, even after the Examiner's combination the resulting reference does not suggest all of the claim elements. Therefore, the Examiner fails to make out a prima facie case of obviousness.

# H. REFERENCES DO NOT SUGGEST OR TEACH MOTIVATION TO COMBINE

For argument sake, even if Cassidy et al., the primary reference, did suggest elements of claim 1 and/or claim 16<sup>1</sup> except for the dividing step which the Examiner admits is not taught by Cassidy, et al. and relies on Steven B. Wicker for teaching this element, it is applicants' contention the combination would be improper in that there is no motivation in either of these references to form the combination. As argued above and incorporate herein by reference, Cassidy et al. uses a table of prerecorded CRC values in combination with a logical grid to quickly determine an appropriate CRC value. Wicker suggests dividing a generator polynomial GX into a message polynomial. The method of calculating CRC in Cassidy does not lend itself to this dividing step. Therefore, applicants contend if Cassidy is amended to include the division set forth in Wicker, Cassidy's method of calculating the CRC would be destroyed. Any modification that destroys the basis of an invention is, in fact, evidence of non-motivation suggestion.

<sup>&</sup>lt;sup>1</sup>A proposition to which applicants disagree, see arguments traversing in G. above.

PATENT IBM Docket No. FR920010006US1

Moreover, applicants argue the skill and knowledge required to incorporate the teachings in Wicker with Cassidy would be too complex and far beyond the reach of an artisan.

Even though none of the references suggest a motivation to combine the claim could still be obvious if the Examiner set forth logical and concrete reasons why an artisan viewing these references would combine them in such a way to render the claim obvious. The argument for combination set forth by the Examiner is on page 12 of the Office Action. It is applicants' contention that the reason provided as basis for the combination does not appear to be logical or concrete. Therefore, the Examiner has not presented a prima facie case of obviousness.

Furthermore, applicants argue the process steps set forth in applicants' claims are novel. Because, as argued above and incorporated herein by reference at least one element of claim 1 and claim 16 is not found in the cited reference. In addition, applicants' invention set forth a generic method to compute a CRC on a bit chain of any length having any generator polynomial using a device a few components including a divider, an adder. register and multiplier (see Fig. 5). The simplicity of this circuit is regarded as benefit to the user. The novel process step and benefits are indicia of unobviousness. As a consequence the claims are not obvious in view of the teaching of the references.

The dependent claims are also unobvious for reasons set forth above.

Claim 5 is rejected under 35 USC 103(a) as being unpatentable over Cassidy (U.S. Patent 6,684,363 B1) and Wicker (Steven B. Wicker, "Error control system for digital communication storage" Princess Hall, 1995, pages 116-121) in view of Freeman et al. (U.S. Patent 3,678,469).

PATENT IBM Docket No. FR920010006US1

In response, applicants respectfully traverse the rejection and argue claim 5 is not obvious for reasons set forth herein. Claim 5 by reason of dependency on claim 1 inherit the elements recited therein. As argued above and incorporated herein by reference the combination of Cassidy and Wicker does not render claim 1 obvious and likewise would not render claim 5 obvious. The Freeman et al. reference (U.S. Patent 3,678,469) does not disclose the deficiency set forth relative to Cassidy and Wicker. Therefore, the Freeman et al. reference is merely cumulative and when combined with Wicker and Cassidy would not render claim 5 obvious.

Claim 7 is rejected under 35 USC 103(a) as being unpatentable over Cassidy (U.S. Patent 6,684,363 B1) and Wicker (Steven B. Wicker, "Error control system for digital communication storage" Princess Hall, 1995, pages 116-121) in view of Kanasugi et al. (U.S. Patent 6,493,844).

Applicants respectfully traverse the rejection and argue for reasons set forth herein claim 7 is not obvious in view of the teachings of the references. Claim 7 by reason of dependency on claim 1 inherits all the elements of that claim. As argued above and incorporated herein by reference the combination of Cassidy et al. and Wicker et al. do not render claim 1 obvious. For the same reasoning they would not render the dependent claim 7 obvious. The Kanasugi reference (U.S. Patent 6,493,844) does not provide the deficiencies that were argued relative to Cassidy and Wicker. Therefore, in this regard the Kanasugi reference is merely cumulative and when combined with Wicker and Cassidy do not render claim 7 obvious.

Newly added claim 19 is also patentable over the art of record for reasons set forth above and incorporated herein by reference.

PATENT IBM Docket No. FR920010005031

It is believed that the present amendment answers all the issues raised by the Examiner. Reconsideration is hereby requested and an early allowance of all the claims is solicited.

Respectfully Submitted,

Joscelyn G. Cockburn

Attorney of Record, Reg. No. 27,069

Customer No. 25299 IBM Corporation

Dept 9CCA/002; P.O. Box 12195

Research Triangle Park, NC 27709-2195

Phone: (919) 543-9036 / FAX: (919) 254-2649